CLAIMS

What is claimed is:

1. A method of implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the method comprising:

generating an unrouted logic placement for the design;

routing the unrouted logic placement to produce a routed design; and

modifying the routed design to reduce susceptibility of the design to the SEUs.

2. The method of Claim 1, wherein the PLD is a field programmable gate array (FPGA).

3. The method of Claim 1, wherein the design comprises source logic, destination logic, and a node coupled between the source logic and the destination logic, and wherein modifying the routed design comprises providing duplicate routing paths for the node.

4. The method of Claim 3, wherein the duplicate routing paths traverse a programmable routing multiplexer in the PLD, and wherein an SEU affecting input selection for the programmable routing multiplexer changes the input selection from one to another of the duplicate routing paths.

5. The method of Claim 4, wherein:

generating an unrouted logic placement for the design comprises assigning the source logic to a first logic block in the PLD and assigning the destination logic to a second logic block in the PLD; and

modifying the routed design comprises:

identifying first and second data input terminals of a programmable routing multiplexer in the PLD, wherein a selection between the first and second data input terminals is determined by a value stored in a memory cell controlling the programmable routing multiplexer;

routing the node on a first routing path between the first and second logic blocks, wherein the first routing path traverses the programmable routing multiplexer via the first data input terminal; and

routing the node on a second routing path between the first and second logic blocks, wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal.

6. The method of Claim 5, wherein the PLD is a field programmable gate array (FPGA), and wherein the memory cell is a static RAM-based configuration memory cell of the FPGA.

7. The method of Claim 3, further comprising:

evaluating the source and destination logic and determining that the source and destination logic do not form a portion of a triple modular redundancy (TMR) circuit.

8. The method of Claim 3, wherein:

generating an unrouted logic placement for the design comprises implementing the destination logic using triple modular redundancy (TMR); and

providing duplicate routing paths for the node comprises providing three routing paths for the node, each of the three routing paths providing one TMR input signal to the destination logic.

9. The method of Claim 8, wherein:

the PLD is a field programmable gate array (FPGA) comprising a look-up table (LUT); and

generating an unrouted logic placement for the design further comprises synthesizing the design to ensure that the destination logic has two fewer input signals than the LUT.

10. The method of Claim 8, wherein:

the PLD is a field programmable gate array (FPGA) comprising a look-up table (LUT) having N input terminals, where N is an integer at least equal to four;

the destination logic implements a function having no more than N-2 inputs, of which one input is provided by the node; and

implementing the destination logic using TMR comprises implementing the destination logic in the LUT, three of the input terminals of the LUT being coupled to the three routing paths for the node.

11. The method of Claim 3, wherein the duplicate routing paths comprise a first path traversing a transparent latch and a second path bypassing the transparent latch.

12. The method of Claim 11, wherein the PLD is a field programmable gate array (FPGA), and wherein the transparent latch comprises a programmable memory element in the FPGA configured as a transparent latch.

13. The method of Claim 3, wherein the destination logic comprises a logic gate having a plurality of input terminals each coupled to one of the duplicate routing paths and further coupled to a weak pull-up, the logic gate comprising one of an AND and a NAND gate.

14. The method of Claim 3, wherein the destination logic comprises a logic gate having a plurality of input terminals each coupled to one of the duplicate routing paths and further coupled to a weak pull-down, the logic gate comprising one of an OR and a NOR gate.

15. A computer-readable storage medium comprising computer-executable code for implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the medium comprising:

code for generating an unrouted logic placement for the design;

code for routing the unrouted logic placement to produce a routed design; and

code for modifying the routed design to reduce susceptibility of the design to the SEUs.

16. The medium of Claim 15, wherein the PLD is a field programmable gate array (FPGA).

17. The medium of Claim 15, wherein the design comprises source logic, destination logic, and a node coupled between the source logic and the destination logic, and wherein the code for modifying the routed design comprises code for providing duplicate routing paths for the node.

18. The medium of Claim 17, wherein the duplicate routing paths traverse a programmable routing multiplexer in the PLD, and wherein an SEU affecting input selection for the programmable routing multiplexer changes the input selection from one to another of the duplicate routing paths.

19. The medium of Claim 17, further comprising:

code for evaluating the source and destination logic and determining that the source and destination logic do not form a portion of a triple modular redundancy (TMR) circuit.

20. The medium of Claim 17, wherein:

the code for generating an unrouted logic placement for the design comprises code for implementing the destination logic using triple modular redundancy (TMR); and

the code for providing duplicate routing paths for the node comprises code for providing three routing paths for the node, each of the three routing paths providing one TMR input signal to the destination logic.

21. The medium of Claim 20, wherein:

the PLD is a field programmable gate array (FPGA) comprising a look-up table (LUT); and

the code for generating an unrouted logic placement for the design further comprises code for synthesizing the design to ensure that the destination logic has two fewer input signals than the LUT.

22. The medium of Claim 20, wherein:

the PLD is a field programmable gate array (FPGA) comprising a look-up table (LUT) having N input terminals, where N is an integer at least equal to four;

the destination logic implements a function having no more than N-2 inputs, of which one input is provided by the node; and

the code for implementing the destination logic using TMR comprises code for implementing the destination logic in the LUT, three of the input terminals of the LUT being coupled to the three routing paths for the node.

23. The medium of Claim 17, wherein the duplicate routing paths comprise a first path traversing a transparent latch and a second path bypassing the transparent latch.

24. The medium of Claim 23, wherein the PLD is a field programmable gate array (FPGA), and the transparent latch comprises a programmable memory element in the FPGA configured as a transparent latch.

25. The medium of Claim 17, wherein the destination logic comprises a logic gate having a plurality of input terminals each coupled to one of the duplicate routing paths and further coupled to a weak pull-up, the logic gate comprising one of an AND and a NAND gate.

26. The medium of Claim 17, wherein the destination logic comprises a logic gate having a plurality of input terminals each coupled to one of the duplicate routing paths and further coupled to a weak pull-down, the logic gate comprising one of an OR and a NOR gate.

27. A computer system for implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the computer system comprising:

a placement module for generating an unrouted logic placement for the design;

a first routing module for routing the unrouted logic placement to produce a routed design; and

a second routing module for modifying the routed design to reduce susceptibility of the design to the SEUs.

28. The computer system of Claim 27, wherein the PLD is a field programmable gate array (FPGA).

29. The computer system of Claim 27, wherein the design comprises source logic, destination logic, and a node coupled between the source logic and the destination logic, and wherein the second routing module provides duplicate routing paths for the node.

30. A method of implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the design comprising source logic, destination logic, and a node coupled between the source logic and the destination logic, the method comprising:

generating an unrouted logic placement for the design; and

routing the unrouted logic placement to produce a routed design including duplicate routing paths for the node.

31. The method of Claim 30, wherein the PLD is a field programmable gate array (FPGA).

32. The method of Claim 30, wherein the duplicate routing paths traverse a programmable routing multiplexer in the PLD, and wherein an SEU affecting input selection for the programmable routing multiplexer changes the input selection from one to another of the duplicate routing paths.

33. The method of Claim 30, wherein:

generating an unrouted logic placement for the design comprises assigning the source logic to a first logic block in the PLD and assigning the destination logic to a second logic block in the PLD; and

routing the unrouted logic placement comprises:

identifying first and second data input terminals of a programmable routing multiplexer in the PLD, wherein a selection between the first and second data input terminals is determined by a value stored in a memory cell controlling the programmable routing multiplexer;

routing the node on a first routing path between the first and second logic blocks, wherein the first routing path traverses the programmable routing multiplexer via the first data input terminal; and

routing the node on a second routing path between the first and second logic blocks, wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal.

34. The method of Claim 33, wherein the PLD is a field programmable gate array (FPGA), and wherein the memory cell is a static RAM-based configuration memory cell of the FPGA.

35. The method of Claim 30, further comprising:

evaluating the source and destination logic and determining that the source and destination logic do not form a portion of a triple modular redundancy (TMR) circuit.

36. The method of Claim 30, wherein:

generating an unrouted logic placement for the design comprises implementing the destination logic using triple modular redundancy (TMR); and

the duplicate routing paths comprise three routing paths for the node, each of the three routing paths providing one TMR input signal to the destination logic.

37. The method of Claim 36, wherein:

the PLD is a field programmable gate array (FPGA) comprising a look-up table (LUT); and

generating an unrouted logic placement for the design further comprises synthesizing the design to ensure that the destination logic has two fewer input signals than the LUT.

38. The method of Claim 36, wherein:

the PLD is a field programmable gate array (FPGA) comprising a look-up table (LUT) having N input terminals, where N is an integer at least equal to four;

the destination logic implements a function having no more than N-2 inputs, of which one input is provided by the node; and

implementing the destination logic using TMR comprises implementing the destination logic in the LUT, three of the input terminals of the LUT being coupled to the three routing paths for the node.

39. The method of Claim 30, wherein the duplicate routing paths comprise a first path traversing a transparent latch and a second path bypassing the transparent latch.

40. The method of Claim 39, wherein the PLD is a field programmable gate array (FPGA), and wherein the transparent latch comprises a programmable memory element in the FPGA configured as a transparent latch.

41. The method of Claim 30, wherein routing the unrouted logic placement comprises:

selecting input terminals of the multiplexer to maximize a number of duplicate paths differing by a single select bit; and

routing the duplicate paths through the selected input terminals of the multiplexer.

42. The method of Claim 30, wherein the destination logic comprises a logic gate having a plurality of input terminals each coupled to one of the duplicate routing paths and further coupled to a weak pull-up, the logic gate comprising one of an AND and a NAND gate.

43. The method of Claim 30, wherein the destination logic comprises a logic gate having a plurality of input terminals each coupled to one of the duplicate routing paths and further coupled to a weak pull-down, the logic gate comprising one of an OR and a NOR gate.

44. A computer-readable storage medium comprising computer-executable code for implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the medium comprising:

code for generating an unrouted logic placement for the design; and

code for routing the unrouted logic placement to produce a routed design including duplicate routing paths for the node.

45. The medium of Claim 44, wherein the PLD is a field programmable gate array (FPGA).

46. The medium of Claim 44, wherein the duplicate routing paths traverse a programmable routing multiplexer in the PLD, and wherein an SEU affecting input selection for the programmable routing multiplexer changes the input selection from one to another of the duplicate routing paths.

47. The medium of Claim 44, further comprising:

code for evaluating the source and destination logic and determining that the source and destination logic do not form a portion of a triple modular redundancy (TMR) circuit.

48. The medium of Claim 44, wherein:

the code for generating an unrouted logic placement for the design comprises code for implementing the destination logic using triple modular redundancy (TMR); and

the duplicate routing paths comprise three routing paths for the node, each of the three routing paths providing one TMR input signal to the destination logic.

49. The medium of Claim 48, wherein:

the PLD is a field programmable gate array (FPGA) comprising a look-up table (LUT); and

the code for generating an unrouted logic placement for the design further comprises code for synthesizing the design to ensure that the destination logic has two fewer input signals than the LUT.

50. The medium of Claim 48, wherein:

the PLD is a field programmable gate array (FPGA) comprising a look-up table (LUT) having N input terminals, where N is an integer at least equal to four;

the destination logic implements a function having no more than N-2 inputs, of which one input is provided by the node; and

the code for implementing the destination logic using TMR comprises code for implementing the destination logic in the LUT, three of the input terminals of the LUT being coupled to the three routing paths for the node.

51. The medium of Claim 44, wherein the duplicate routing paths comprise a first path traversing a transparent latch and a second path bypassing the transparent latch.

52. The medium of Claim 51, wherein the PLD is a field programmable gate array (FPGA), and wherein the transparent latch comprises a programmable memory element in the FPGA configured as a transparent latch.

53. The medium of Claim 44, wherein the code for routing the unrouted logic placement comprises:

code for selecting input terminals of the multiplexer to maximize a number of duplicate paths differing by a single select bit; and

code for routing the duplicate paths through the selected input terminals of the multiplexer.

54. The medium of Claim 44, wherein the destination logic comprises a logic gate having a plurality of input terminals each coupled to one of the duplicate routing paths and further coupled to a weak pull-up, the logic gate comprising one of an AND and a NAND gate.

55. The medium of Claim 44, wherein the destination logic comprises a logic gate having a plurality of input terminals each coupled to one of the duplicate routing paths and further coupled to a weak pull-down, the logic gate comprising one of an OR and a NOR gate.

56. A computer system for implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the computer system comprising:

a placement module for generating an unrouted logic placement for the design; and

a routing module for routing the unrouted logic placement to produce a routed design including duplicate routing paths for the node.

57. The computer system of Claim 56, wherein the PLD is a field programmable gate array (FPGA).

58. A configuration data file implementing in a programmable logic device (PLD) a design having reduced susceptibility to single-event upsets (SEUs), the design comprising source logic, destination logic, and a node coupled between the source logic and the destination logic, the configuration data file comprising:

configuration data assigning the source logic to a first logic block in the PLD;

configuration data assigning the destination logic to a second logic block in the PLD;

configuration data implementing the node as a first routing path between the first and second logic blocks; and

configuration data implementing the node as a second routing path between the first and second logic blocks.

59. The configuration data file of Claim 58, wherein the PLD is a field programmable gate array (FPGA).

60. The configuration data file of Claim 58, wherein the first and second routing paths traverse a programmable routing multiplexer in the PLD, and wherein an SEU affecting input selection for the programmable routing multiplexer changes the input selection from one to another of the first and second routing paths.

61. The configuration data file of Claim 58, further comprising:

configuration data implementing the destination logic using triple modular redundancy (TMR); and

configuration data implementing the node as a third routing path between the first and second logic blocks.

62. The configuration data file of Claim 61, wherein:

the PLD is a field programmable gate array (FPGA) comprising a look-up table (LUT) having N input terminals, where N is an integer at least equal to four;

the destination logic implements a function having no more than N-2 inputs, of which one input is provided by the node; and

the configuration data implementing the destination logic comprises configuration data implementing the destination logic in the LUT, three of the input terminals of the LUT being coupled to the first, second, and third routing paths.

63. The configuration data file of Claim 58, wherein the first routing path traverses a transparent latch and the second path bypasses the transparent latch.

64. The configuration data file of Claim 63, wherein the PLD is a field programmable gate array (FPGA), the configuration data file further comprising:

configuration data configuring a programmable memory element in the FPGA as the transparent latch.